REMARKS/ARGUMENTS

Favorable reconsideration of this application, in light of the following discussion, is respectfully requested.

Claims 1-19 are pending; Claims 2-5, 7-10 and 12-15 have been withdrawn; and no claims have been newly added, amended, or cancelled herewith.

In the outstanding Office Action, Claim 1 was rejected under 35 U.S.C. § 103(a) as unpatentable over Hara (U.S. Pat. No. 5,202,655), in view of Millman (Micro electronics: Digital and Analog Circuit Systems). Claims 6, 11, and 16-19 were indicated as allowable.

Applicant acknowledges with appreciation the indication that Claims 6, 11, and 16-19 contain allowable subject matter. However, since Claim 1 has not been amended herewith, those claims remain in dependent form.

Regarding the rejection of Claim 1 under 35 U.S.C. § 103(a) as unpatentable over Hara in view of Millman, that rejection is traversed. Claim 1 recites: "an active inductor comprising first and second field effect transistors . . . said gate and said source of second field effect transistor serve as two ports of said active inductor." The claimed configuration enables the minimization of loss and a broad band of inductance.[1]

With reference to Figure 2 of Hara, an admittance matrix when a source and a drain of a FET 15 are interchanged is calculated to determine whether the circuit works as a pseudo gyrator. In Figure 2 of Hara, an electric potential of a terminal with which a resistance 17, a drain of a FET 14, and a gate of a FET 15 are connected is given a reference number Vx, and an electric potential of a terminal with which a source of a FET 44 and a drain of a FET 16 are connected is given a reference number Vy. C_{gs} and g_m of the FETs 14 and 15 are

[1] Specification, page 7, lines 8-11.

assumed to be the same, and are denoted by C_{gsa} and g_{ma}, respectively. C_{gs} and g_m of the FETs 44 and 16 are assumed to be the same, and are denoted by C_{gsb} and g_{mb}, respectively. Further, a current and a voltage of a terminal on the left side of a pseudo gyrator circuit 30 are given reference numbers I_1, V_1, respectively, and a current and a voltage of a terminal on the right side of the pseudo gyrator circuit 30 are given reference numbers I_2, V_2, respectively.

In a node N1, according to the Kirchhoff's current conservation law,

$$I_1 = j\omega C_{gsa} V_1 + g_{mb}(0 - V_y) \quad . \tag{1}$$

In a node of electric potential Vx, according to the Kirchoff's current conservation law,

$$g_{ma} V_1 + \frac{Vx}{R} + j\omega C_{gsa}(Vx - V_2) = 0 \quad . \tag{2}$$

In a node N2 (a nodal point where a gate of a FET 16 and a source of a FET 15 connect with each other), according to the Kirchhoff's current conservation law,

$$I_2 + (g_{ma} + j\omega C_{gsa})(Vx - V_2) = j\omega C_{gsb} V_2 \quad . \tag{3}$$

In a node of electric potential Vy, according to the Kirchhoff's current conservation law,

$$(g_{mb} + j\omega C_{gsb})(0 - Vy) = g_{mb} V_2 \quad . \tag{4}$$

Vy as obtained from the expression (4),

$$Vy = \frac{-g_{mb}}{g_{mb} + j\omega C_{gsb}} V_2 \quad . \tag{5}$$

I_1 as obtained by assigning by expression (5) into the expression (1),

$$I_1 = j\omega C_{gsa} V_1 + \frac{g_{mb}^2}{g_{mb} + j\omega C_{gsb}} V_2 \quad . \tag{6}$$

(Vx-V_2) as obtained from the expression (2),

$$Vx - V_2 = \frac{-g_{ma}R}{1 + j\omega C_{gsa}R}V_1 - \frac{1}{1 + j\omega C_{gsa}R}V_2 \ . \tag{7}$$

I_2 as obtained by assigning the expression (7) into the expression (3),

$$I_2 = \frac{g_{ma}R(g_{ma} + j\omega C_{gsa})}{1 + j\omega C_{gsa}R}V_1 + \left[j\omega C_{gsb} + \frac{g_{ma} + j\omega C_{gsa}}{1 + j\omega C_{gsa}R} \right] V_2 \ . \tag{8}$$

The admittance matrix as obtained from the expression (6) and (8) is as follows:

$$\begin{pmatrix} j\omega C_{gsa} & \dfrac{g_{mb}^2}{g_{mb} + j\omega C_{gsb}} \\ \dfrac{g_{ma}R(g_{ma} + j\omega C_{gsa})}{1 + j\omega C_{gsa}R} & j\omega C_{gsb} + \dfrac{g_{ma} + j\omega C_{gsa}}{1 + j\omega C_{gsa}R} \end{pmatrix} . \tag{9}$$

In the expression (9), assuming that the resistance R is small enough to be ignored when compared to C_{gsa}, a matrix element Y_{21} becomes a real number. Further, when a frequency f is sufficiently smaller than a cutoff frequency f_t, a matrix element Y_{12} becomes a real number. However, because the matrix element Y_{21} is of positive sign and components other than a capacity component $j\omega C_{gsb}$ are inserted into the matrix element Y_{22} in parallel, the admittance matrix no longer shows a gyrator characteristic even if the capacities C_{gsa} and C_{gsb} are connected with both ends of the circuit. Accordingly, because the circuit 30 shown in Figure 2 of Hara does not work as an inductor if a source and a drain of the FET 15 are interchanged, it can be concluded that the circuit 30 of Hara is not ***a two-port element***. Therefore, it is respectfully submitted that Hara fails to disclose or suggest "an active inductor comprising first and second field effect transistors . . . said gate and said source of second field effect transistor serve as ***two ports*** of said active inductor" (emphasis added), as recited in Claim 1.

The Office Action relies on Millman for the concept that the source and drain may be interchangeable. However, the cited portion of Millman also does not disclose or suggest

"said gate and said source of said field effect transistor serve as two ports of said active inductor," and thus Millman does not overcome the above-noted deficiencies in Hara.

Accordingly, as neither Hara or the cited portion of Millman, either alone or in combination, discloses or suggests the features recited in pending independent Claim 1, it is respectfully submitted that the Office Action has failed to provide a *prima facie* case of obviousness. It is therefore respectfully requested that this rejection be withdrawn.

Consequently, in view of the foregoing discussion, it is respectfully submitted that this application is in condition for allowance. An early and favorable action is therefore respectfully requested.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER, & NEUSTADT, P.C.

Surinder Sachar

Gregory J. Maier
Registration No. 25,599
Surinder Sachar
Registration No. 34,423
Attorneys of Record

22850
Tel.: (703) 413-3000
Fax: (703) 413-2220
GJM/SNS/KDP/cja/dmr
I:\ATTY\KDP\20'S\204720US\204720US-AFTER FINAL.DOC